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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,468	03/01/2004	Junichi Yanagihara	031948-9	9233

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EXAMINER	
WELLS, KENNETH B	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,468	YANAGIHARA, JUNICHI	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 21-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,21-26 and 30-32* is/are rejected.

7)☒ Claim(s) *27-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Applicant's appeal brief filed on 10/2/06 has been received and entered in the case. In view of the arguments included therein, additional prior art is now cited to support and amplify the previously set forth rejections.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-3, 21 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Altmann.

See paragraph three of the office action mailed on 3/1/06 for the details of this rejection. Also note that the limitation that the current source supplies a first current to the common node is met by Altmann because the current source FETs 115 do in fact supply current to the common node (the commonly-connected sources of FETs M1 and M2), when the FETs M1 and M2 turn on, i.e., when FET M1 turns on current through the lefthand FET 115 is supplied to the common node. As to the limitation that the comparison circuit compares currents, note that Altmann's comparison circuit (amplifier A(s) in combination with circuit 120) compares the current flowing in circuit 120 with a current corresponding to voltage CM ref, which corresponds to applicant's comparison circuit 10 which compares

first and second voltages that are derived from first and second currents.

4. Claims 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Altmann in view of either Watarai or Wu.

As to claim 30, the details of the controller do not patentably distinguish over Altmann because such a circuit for supplying a differential input signal is old and well-known, as shown by each of the above-noted secondary references (see Fig. 7 of Watarai and Fig.2 of Wu). The motivation for using the controller circuits of the secondary references is simply to provide an input circuit that has the advantages taught by these two secondary references. For example, the ability to apply the differential input or cut it off when it is not needed (via action of the enable control input).

As to claims 31 and 32, the limitation that the first and second switch circuits are PMOS transistors does not patentably distinguish over Altmann because a person having ordinary skill in the art will easily recognize that the Altmann Fig. 1 circuit can be implemented using opposite conductivity FETs, i.e., replacing the PFETs with NFETs and vice-versa is a well-known modification to any IC circuit, and such would result in a complemented circuit with differentially-coupled PMOS

transistors receiving in and inb, NMOS transistors in place of FETs 115, and PMOS transistors for FETs M3 and M4. Such a circuit would read on the claim 31 and claim 32 circuitry and thus these two claims also fail to define patentably over Altmann.

5. Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Altmann.

As to claims 23 and 24, the limitations that the first and second switch circuits are PMOS transistors and the current adjustment circuit is also a PMOS transistor do not patentably distinguish over Altmann because a person having ordinary skill in the art will easily recognize that the Altmann Fig. 1 circuit can be implemented using opposite conductivity FETs, i.e., replacing the PFETs with NFETs and vice-versa is a well-known modification to any IC circuit, and such would result in a complemented circuit with differentially-coupled PMOS transistors receiving in and inb, NMOS transistors in place of FETs 115, and PMOS transistors for FETs M3 and M4. Such a circuit would read on the claim 23 and claim 24 circuitry and thus these two claims also fail to define patentably over Altmann.

As to claim 25, it is old and well-known in the art that

reference voltages such as CM ref in Altmann's Fig. 1 are typically formed when a reference current flows through a load element or elements, of which fact official notice is taken by the examiner. Thus, claim 25 does not patentably distinguish over Altmann.

As to claim 26, FETs 115 and the load (current source) FETs within circuit 120 are "proportional" to the extent that this term can be broadly interpreted to mean that these FETs are all the same size (i.e., the term "proportional" does not necessarily mean different in size, and thus two FETs of equal size can be considered "proportional" to each other).

6. Claims 27-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As further allowable subject matter, it is noted that claim 1 would be allowable if it were amended to recite, on line 2, that the current source is connected directly to the common node. Claim 21 also would be allowable if it were amended to recite, on line 2, that the first transistor is connected directly to the first node.

8. Applicant's arguments filed on 10/2/06 have been fully considered but they are not persuasive.

The argument that either of the two constantly-biased FETs 115 in Altmann's Fig. 1 cannot be interpreted as a current source is not persuasive because it is common terminology in the semiconductor IC art to refer to constantly-biased FETs that are connected between a high power supply (e.g., Vcc) and a pair of differentially-connected transistors as "current source loads", see for example, Fig. 3 of Cheng, U.S. patent no. 5,798,660 (where FETs P1 and P4 are described as current source loads). Note further Fig. 1a of Lee, U.S. patent no. RE36,013 (where the load elements between Vdd and the differentially-connected transistors are likewise described as current source loads). Thus, applicant's argument that the FETs 115 in Fig. 1 of Altmann cannot be interpreted as current sources is without merit.

The further argument, that in Altmann's Fig. 1 the constantly-biased FETs within circuit 120 do not perform "mirroring" of the current flowing through FETs 115, is similarly not persuasive because the structure is the same as in the instant invention. In other words, applicant's mirroring involves the PMOS transistor 2 receiving the same bias voltage as the PMOS transistor 23 in order to effect the mirroring, and

Altmann's mirroring also involves the same bias potential being received by the FETs 115 and the PMOS transistors within circuit 120 to likewise effect current mirroring. Thus, applicant's argument that the second current in Altmann is not formed by mirroring the first current is also without merit.

9. In view of the above-noted newly cited prior art added to the previous rejections based on Altmann, this action is non-final.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth B. Wells
Primary Examiner
Art Unit 2816

October 28, 2006